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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,544	07/22/2003	Shinya Fujioka	108397-00106	4872

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EXAMINER	
YOHA, CONNIE C	
ART UNIT	**PAPER NUMBER**
2818	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,544	FUJIOKA, SHINYA	
	Examiner	Art Unit	
	Connie C. Yoha	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Examiner took notice of the remarks and amendments made by applicant filed on 9/02/04.

2. A second non-final rejection is applied to the pending claims using newly cited reference.

Response to Amendment

3. This office action is in response to Amendment filed on 9/02/04.

Claim 52, 55, and 56 are amended.

Claims 1-43 are canceled.

4. Claims 44-56 are pending.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 44-48 are rejected under 35 U.S.C. 102(b) as being anticipated by Hoenigschmide et al, Pat. No. 5970009.

With regard to claim 44, Hoenigschmide discloses a method of operating a semiconductor memory including dynamic memory cells comprising the step of: entering a low power consumption mode (standby mode), in which the dynamic memory cells do not retain data therein by prohibiting refresh operations (col. 1, line 27-33), in response to a dedicated external control signal (col. 1, line 56-62).

With regard to claim 45, Hoenigschmide discloses the memory enters the low power consumption mode in response to a voltage change of the dedicated external control signal from a first voltage (1.75V) to a second voltage (1.0V) (col. 3, line 46-54).

With regard to claim 46, Hoenigschmide discloses wherein the low power consumption mode is maintained while the dedicated external control signal has the second voltage (col. 3, line 46-54).

With regard to claim 47, wherein the memory exits the low power consumption mode in response to a reverse voltage change of the dedicated external control signal from the second voltage to the first voltage (col. 3,line 52-59) (col. 3, line 65-col. 4, line 2).

With regard to claim 48, Hoenigschmide discloses method of controlling a semiconductor memory including dynamic memory cells, comprising the step of: outputting a dedicated control signal to the memory so that the memory enters a low power consumption mode (col. 1, line 54-62), in which the dynamic memory cells do not retain data therein by prohibiting refresh operation (col. 1, line 29-33).

With regard to claim 49, Hoenigschmide further discloses the step of keeping the voltage of the dedicated control signal at the second voltage to maintain the low power consumption mode of the semiconductor memory (col. 3,line 46-54).

With regard to claim 51, Hoenigschmide further discloses step of changing the voltage of the dedicated control signal from the second voltage to the first voltage so that the semiconductor memory exists the low power consumption mode (col. 3, line 52-59) (col. 3, line 65-col. 2, line 2).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 52-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hoenigschmide et al, Pat. No. 5970009 in view of Soini et al, Pat. No. 6445932..

With regard to claim 52, Hoenigschmide discloses a memory system comprising: a first memory including dynamic memory cells (DRAM) having a low power consumption mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operation (col. 1, line 29-33) and the first memory

having a data terminal (col. 2, line 25-27). Hoenigschmide, does not discloses a second memory including flash memory cells, However, Hoenigschmide does discloses the invention related to DRAMs having one type of standby mode of operation, whereby it require data to be transfer to a non-volatile memory upon a standby mode and to be restored to its pre-standby mode state when resuming normal operation (col. 2, line 8-15). Soini, however, discloses similar concepts of data transfer between DRAM and nonvolatile memory in a low power consumption mode (Soini, col. 36-41). The nonvolatile being specifically directed as a FLASH type nonvolatile (Soini, col. 9, 40). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to use a flash memory cells as a type of nonvolatile memory to stored data during a low power consumption mode (standby mode or power save mode) as a mean suitable for long time saving as taught by Soini into Hoenigschmide's during power saving mode.

Hoenigschmide also does not explicitly discloses a second memory having a data terminal which is connected with the data terminal of the first memory. However, since the first memory (DRAM) cells and the second memory (nonvolatile -flash) cells conduct transferring of storage data between two (col. 2, line 8-15), it is inherently known to the skill in the art that a second memory data terminal must be connected with the first data memory in order for it to successfully transfer storage data between each other.

With regard to claim 53, Hoenigschmide discloses wherein data stored in the dynamic memory cells in the first memory is transferred to the flash memory cells in the

second memory before the first memory enters the low power consumption mode (col. 2, line 8-15).

With regard to claim 54, Hoenigschmide discloses wherein data stored in the flash memory cells in the second memory is transferred to the dynamic memory cells in the first memory after the first memory exits the low power consumption mode (col. 2,line 8-15).

With regard 55, Hoenigschmide discloses a processing system having a memory first memory including dynamic memory cells, having a low power consumption mode (standby mode) in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operation (col. 1,line 29-33) and the first memory having a data terminal (col. 2, 25-27); and a second memory (nonvolatile) (col. 2, line 12); wherein data stored in the dynamic memory cells in the first memory is transferred to the second memory cells then the first memory enters the low power consumption mode upon shifting from the service state (normal mode) to the waiting state (standby mode) (col. 2, line 8-15), and wherein the first memory exits the low power consumption mode (normal mode) then data stored in the second memory is transferred to the dynamic first memory upon shifting from the waiting state (standby mode) to the service state (normal mode) (col. 2,line 8-15).

First. Hoenigschmide does not discloses a second memory including flash memory cells. Soini, however, discloses similar concepts of data transfer between DRAM and nonvolatile memory in a low power consumption mode (Soini, col. 36-41). The nonvolatile being specifically directed as a FLASH type nonvolatile (Soini, col. 9,

40). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to use a flash memory cells as a type of nonvolatile memory to stored data during a low power consumption mode (standby mode or power save mode) as a mean suitable for long time saving as taught by Soini into Hoenigschmide's during power saving mode.

Secondly, Hoenigschmide also does not explicitly discloses a second memory having a data terminal which is connected with the data terminal of the first memory. However, since the first memory (DRAM) cells and the second memory (nonvolatile - flash) cells conduct transferring of storage data between two (col. 2, line 8-15), it is inherently known to the skill in the art that a second memory data terminal must be connected with the first data memory in order for it to successfully transfer storage data between each other.

Thirdly, Hoenigschmide does not explicitly disclose that a processing systems having the above features are used in a cellular phone having a service state (active mode) and a waiting state (low power mode). However, Soini discloses a multi-service mobile station device having integrated embedded non-volatile (fig. 4, flash) and a volatile memory (fig. 4, DRAM) having a service state (active mode) and a waiting state (low power mode) (col. 9, line 26-53). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to incorporate the used of non-volatile and volatile memory device in a mobile communication device such as cellular phone similar to Soini's into Hoenigschmide's to provide a data processing system which can have the operational advantages of volatile memory device having a

relatively large memory capacity and high operation speed, but with the further advantage of non-volatile retention of data when power are in low consumption mode.

With regard to claim 56, Hoenigschmide discloses a method of controlling a first memory including dynamic memory cells, having a low power consumption mode in which the dynamic memory cells do not retain data therein while power is on by prohibiting refresh operations (col. 1, line 28-33) and a second memory (nonvolatile) (col. 2, line 12), comprising steps of: transferring data stored in the dynamic memory cells in the first memory to the second memory before the first memory enters the low power consumption mode (col. 2, line 11-12); and transferring data stored in the second memory to dynamic memory cells in the first memory after the first memory exits the low power consumption mode (col. 2, line 12-13). Hoenigschmide does not discloses a second memory including flash memory cells. Soini, however, discloses similar concepts of data transfer between DRAM and nonvolatile memory in a low power consumption mode (Soini, col. 36-41). The nonvolatile being specificly directed as a FLASH type nonvolatile (Soini, col. 9, 40). Therefore, it would have been obvious for one having an ordinary skill in the art at the time the invention was made to use a flash memory cells as a type of nonvolatile memory to stored data during a low power consumption mode (standby mode or power save mode) as a mean suitable for long time saving as taught by Soini into Hoenigschmide's during power saving mode.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Hsu (6556477), Sato et al (6515928), Jha et al (6407949), Takasugi (5544096), Yazdy et al (5500827), Cole et al (5241680), Mnich et al (5262998) all disclose a memory device having volatile and nonvolatile memory having mode setting that sets one of the power down or sleep or low power consumption modes.

8. When responding to the office action, Applicants' are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov Should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

October 2004

CONNIE C. YOHA
PRIMARY EXAMINER